DEVELOPMENT OF AN ELECTROPHORETIC IMAGE DISPLAY

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The purpose of this work is to develop a 350 x 600 element X-Y addressed electrophoretic image display (EPID). Devices with improved Mylar layers have been fabricated using the photolithographic masks designed for the 512 character display. This improvement was achieved by using a new system and better pressing blocks. The photolithographic processes and ion-beam milling of the aluminum consistently have given good results. Ion-beam milling of the Mylar requires further development to ensure complete removal of material from the wells without destruction of the underlying electrode

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20. ABSTRACT (Cont'd.)

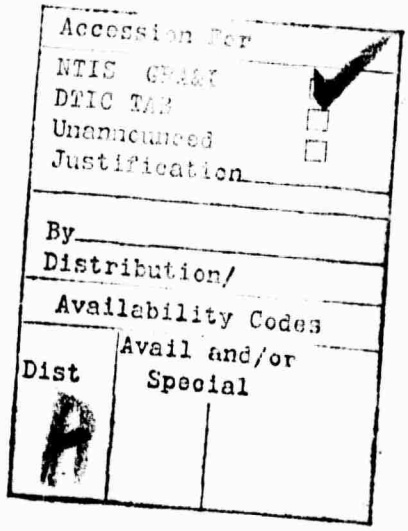
Those areas of the completed devices which operated demonstrated good contrast at 2 lp/mm with the expected drive voltages. The display driver was redesigned to use a new high-voltage shift register for the row and column drivers, and a multiplexer was added to permit future access to any pixel, thereby eliminating the constraints imposed by a character generator. Construction of the driver has begun, and the printed circuit board for mounting the display has been ordered. The system for depositing In_2O_3/SnO_2 (ITO) transparent grid electrodes is in operation. Transparent conducting ITO films have been deposited on glass and Mylar. Additional work is required to establish the deposition parameters necessary for reproducibly obtaining the desired properties of ITO on Mylar.

PREFACE

This work is being performed by Philips Laboratories, a Division of North American Philips Corporation, Briarcliff Manor, New York under the overall supervision of Dr. Barry Singer, Director, Component and Device Research Group. Mr. Richard Liebert, Metallurgist, is the Program Leader; Mr. Joseph Lalak, Electronic Engineer, is responsible for cell fabrication and technology. Mr. Karl Wittig, Electrical Engineer, is responsible for circuit design; Dr. Howard Sorkin, Organic Chemist, has joined the staff and will be responsible for electrophoretic suspensions.

This program is sponsored by the Defense Advanced Research Agency (DARPA) and was initiated under Contract No. MDA903-79-C-0439. Dr. Robert E. Kahn is the Contracting Officer's Technical Representative for DARPA.

The work described in this fourth Quarterly Technical Report covers the period from 1 May 1980 to 31 July 1980.



SUMMARY

The purpose of this work is to develop a 350 x 600 element X-Y addressed electrophoretic image display (EPID). Devices with improved Mylar layers have been fabricated using the photolithographic masks designed for the 512 character display. This improvement was achieved by using a new system and better pressing blocks. The photolithographic processes and ion-beam milling of the aluminum consistently have given good results. Ion-beam milling of the Mylar requires further development to ensure complete removal of material from the wells without destruction of the underlying electrode. Those areas of the completed devices which operated demonstrated good contrast at 2 lp/mm with the expected drive voltages. The display driver was redesigned to use a new high-voltage shift register for the row and column drivers, and a multiplexer was added to permit future access to any pixel, thereby eliminating the constraints imposed by a character generator. Construction of the driver has begun, and the printed circuit board for mounting the display has been ordered. The system for depositing In_2O_3/SnO_2 (ITO) transparent grid electrodes is in operation. Transparent conducting ITO films have been deposited on glass and Mylar. Additional work is required to establish the deposition parameters necessary for reproducibly obtaining the desired properties of ITO on Mylar.

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1. INTRODUCTION

The photolithographic masks for the Phase I display were received and devices have been fabricated and tested. Improvement in the laminating procedure has greatly reduced the defect density in the Mylar layers. The In_2O_3/SnO_2 (ITO) sputtering system is operational and is being characterized. The display driver has been redesigned to incorporate a new high-voltage shift register and a multiplexer. Construction of the driver has begun, and the artwork for the display mounting board has been approved.

2. FABRICATION TECHNOLOGY

2.1 Mylar Sealing

Further improvements have been made in bonding the 12.5 μm thick Mylar to the In_2O_3 row electrode substrate by using a new system. The epoxy layer applied with this new system is much more uniform in thickness, and the number of defects due to particulate contamination is greatly reduced.

The most recent devices were made using the new system and better pressing blocks. The resulting laminates were of excellent quality. There were no voids and very few inclusions in the bond area, and the surface of the Mylar was very smooth and flat. No problems with the adhesion of the aluminum grid electrode to the Mylar as a result of the use of the release agent have been noted.

2.2 Ion-Beam Milling

As noted in the previous quarterly report, it is difficult to remove all the epoxy from the bottom of the wells without completely removing the underlying In_2O_3 electrode in certain areas. Iterative milling and microscopic inspection did not completely alleviate this problem. Therefore, we have added In_2O_3/SnO_2 to the In_2O_3 layer already present, using the newly

grid electrode isolated from the adjacent grid electrodes can be seen. The potential wells are ≈ 13 μm deep, 30 μm wide, 102 μm long and are separated by 6 μm wide walls.

The 512 character devices fabricated during this period could be operated in spite of the faults noted above. Testing of operable portions of the display clearly demonstrated, for the first time, that 2 lp/mm resolution could be obtained in a control grid EPID. Figure 2 is a photo of a portion of a test pattern on the 512 character display. Note that the 0.25 mm square

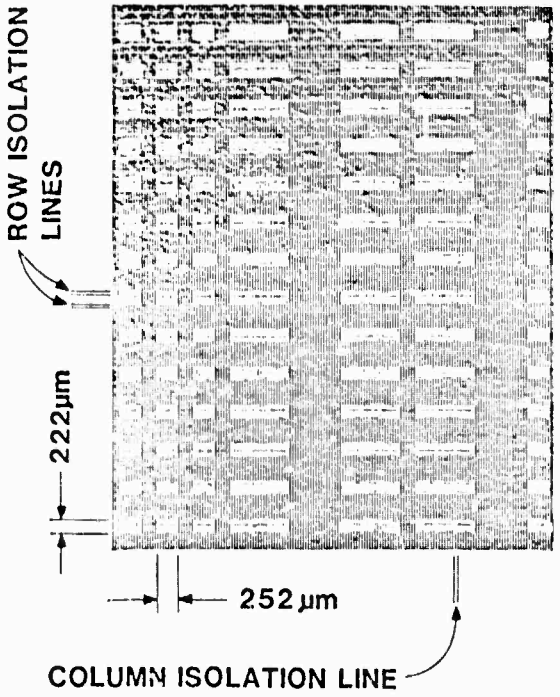

Figure 2. Test pattern demonstrating 2 lp/mm resolution.

pixels are sharply defined. Further note that there is no gap due to column isolation lines between adjacent pixels, and no pigment is trapped in the isolation lines between rows. The electrode potentials necessary to operate this display are within the range expected. With 115 V on the anode, a 15 V difference between the row and column electrodes will hold the pigment in the wells.

Figure 2 also shows the effect of using a highly reflective aluminum-grid electrode and a transparent dielectric. Reflection and diffraction from the grid results in a large

fraction of the ambient light coming from the display to be unmodulated by the presence or absence of pigment in the wells. This effectively reduces the contrast. Replacement of the aluminum with sputtered ITO will result in greatly improved contrast.

2.4 ITO Deposition

The sputtering system for depositing In_2O_3/SnO_2 (ITO) is now in operation. Transparent conducting films of ITO have been deposited on both glass and Mylar at power levels up to 200 W. No post-deposition annealing or deliberate heating of the substrate during deposition has been used. Therefore, the resistivity of these ITO films is about an order of magnitude greater than the best literature values. Since the display requires negligible current for operation, the use of high resistivity electrodes is acceptable.

As mentioned in Section 2.2, ITO is now being used successfully to increase the thickness of the row electrodes. The first samples of ITO on Mylar are being processed, and completed displays with ITO grid electrodes will be ready in September.

2.5 Alternate Epoxy

A test was conducted to evaluate a domestically available epoxy as a replacement for the imported material. After over 1750 hours of testing, we conclude that the replacement is acceptable.

3. DRIVE ELECTRONICS

3.1 Driver Design

Since the last quarterly report, Texas Instruments, Inc. has made available the SN 75501 driver IC. This device was designed for use with plasma displays, and its output drivers are DMOS structures which are capable of switching a potential difference

of up to 100 V. Because of this drive capability, as well as the fact that each IC contains a 32-bit shift register (with each output connected to one driver, and with a serial input), it was decided that these devices could be used as both row and column drivers for the EPID panel.

Since the devices are functionally very similar to the previous column driver IC's (except for the higher output voltage capability and for inputs which can simultaneously make all of the outputs either low or high), the column driving architecture will remain essentially as it was. The row driving architecture, however, was greatly simplified with these devices. Instead of using decoders with drivers connected to their outputs, these same driver IC's can be connected as a long shift register (in a manner similar to the column drivers) in which all of the bits are maintained as logic 1's (output drivers high - unselected condition) except for one logic zero which corresponds to the addressed row, and which propagates along the register to accomplish the scanning of the rows. In both cases, the drivers may be connected directly to the electrodes of the EPID panel with no additional components.

In order to perform the erase function, all of the row drivers can be strobed low, and all of the column drivers can be strobed high, using the appropriate inputs and the respective IC's. Since it is only necessary that both the columns and the rows be at essentially the same potential, which does not have to be any particular value, the function can be accomplished by just bringing all of the columns and all of the rows to their normal select potentials, without using extra circuitry to bring the row drivers to zero volts as was previously done. To perform the set function, the row drivers are simply all strobed high, using the appropriate input on the IC's, while the common anode is pulsed to zero volts. The result is that only two potentials, zero volts and V_{col}, are required for driving the columns, and again only two potentials, V_{ref} aND V_{row}, are required for driving the rows. It is only necessary to reference the row driver IC's to V_{ref}, instead of to ground, in

order for them to perform all of their required driving functions. These IC's can be used as column drivers with no complication.

Figures 3, 4 and 5 show the improved circuit design. Table 1 is the components list. Figure 6 shows how the modular power supplies will be connected to provide power to the IC's and the display. Construction of the drive electronics is in progress.

TABLE 1: Component List.

U1	8748 (Intel) Microprocessor
U2	8291 (Intel) IEEE-488 Interface
U3	RO-3-2513 (GI) 5 x 7 Character Generator
U4,U5	74LS147 Multiplexer
U6	74LS164 P/S Shift Register
U7,U18	SN 75501 (TI) Display Driver
U19,U20	DI 500 (Dionics) Level Shifter
U21	74LS00 Quad NAND Gate
U22,U23	74LS244 Octal Buffer

3.2 Programming the Controller

For possible graphics applications, a multiplexer is used to select whether the input to the parallel-to-serial shift register which in turn feeds the column drivers comes from the ASCII-to-5x7 converter ROM, or from the microprocessor data bus directly. The latter will permit total flexibility.

The 8748 microprocessor software development for the main controller will be done on an IBM System 370 (at the NAPC Data Center), which supports an 8048 assembler and simulator. When it is developed, this software will then be downloaded into an Intel MDS system with an ICE-48 in-circuit emulator. This will, in turn, be connected to the EPID driver in place of the actual microprocessor and used to debug the software and hardware. When this is completed, the MDS prom programmer will be used to burn this software into the internal prom of the 8748, which will be used as the display controller.

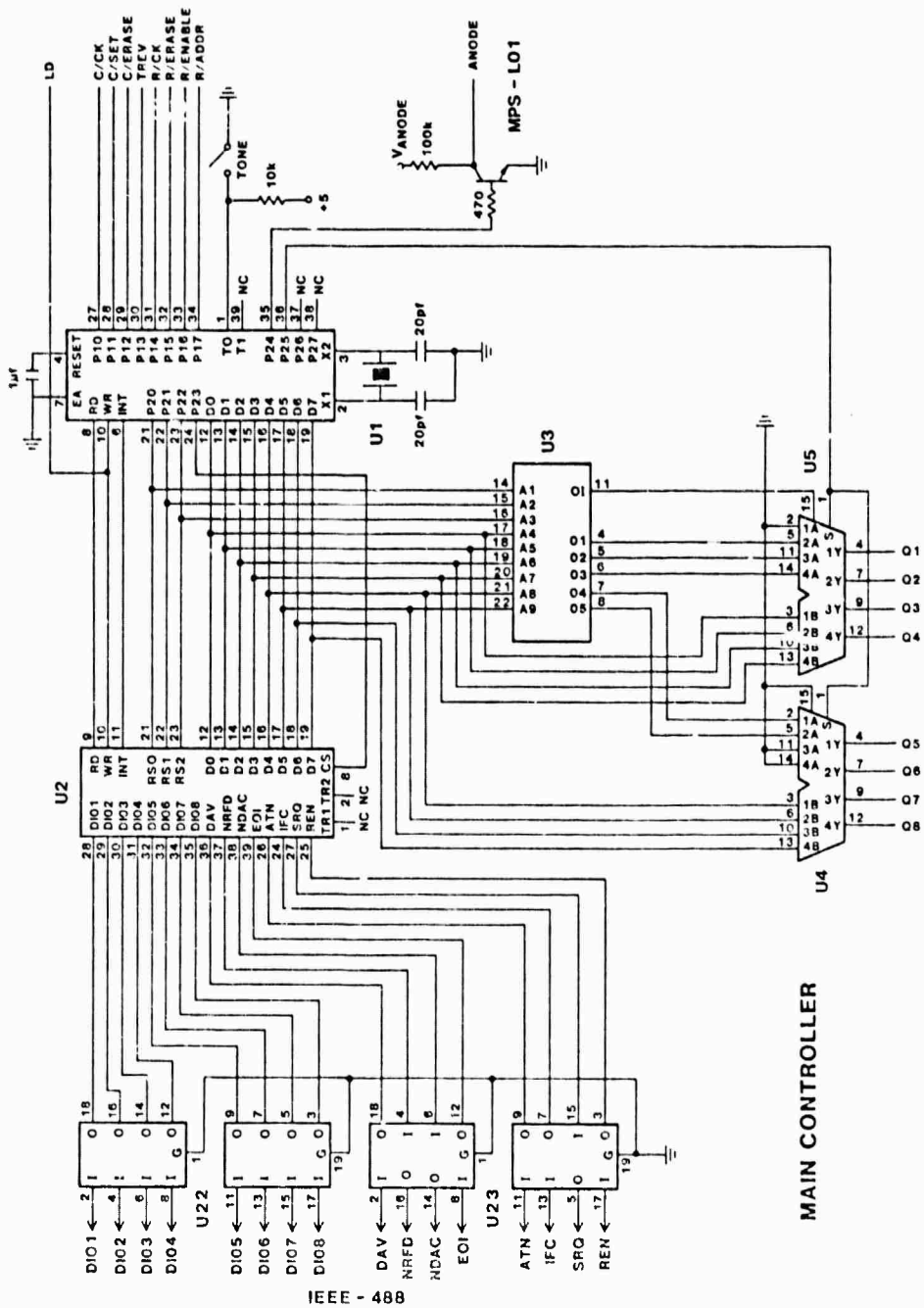

Figure 3. Circuit diagram for interface and controller.

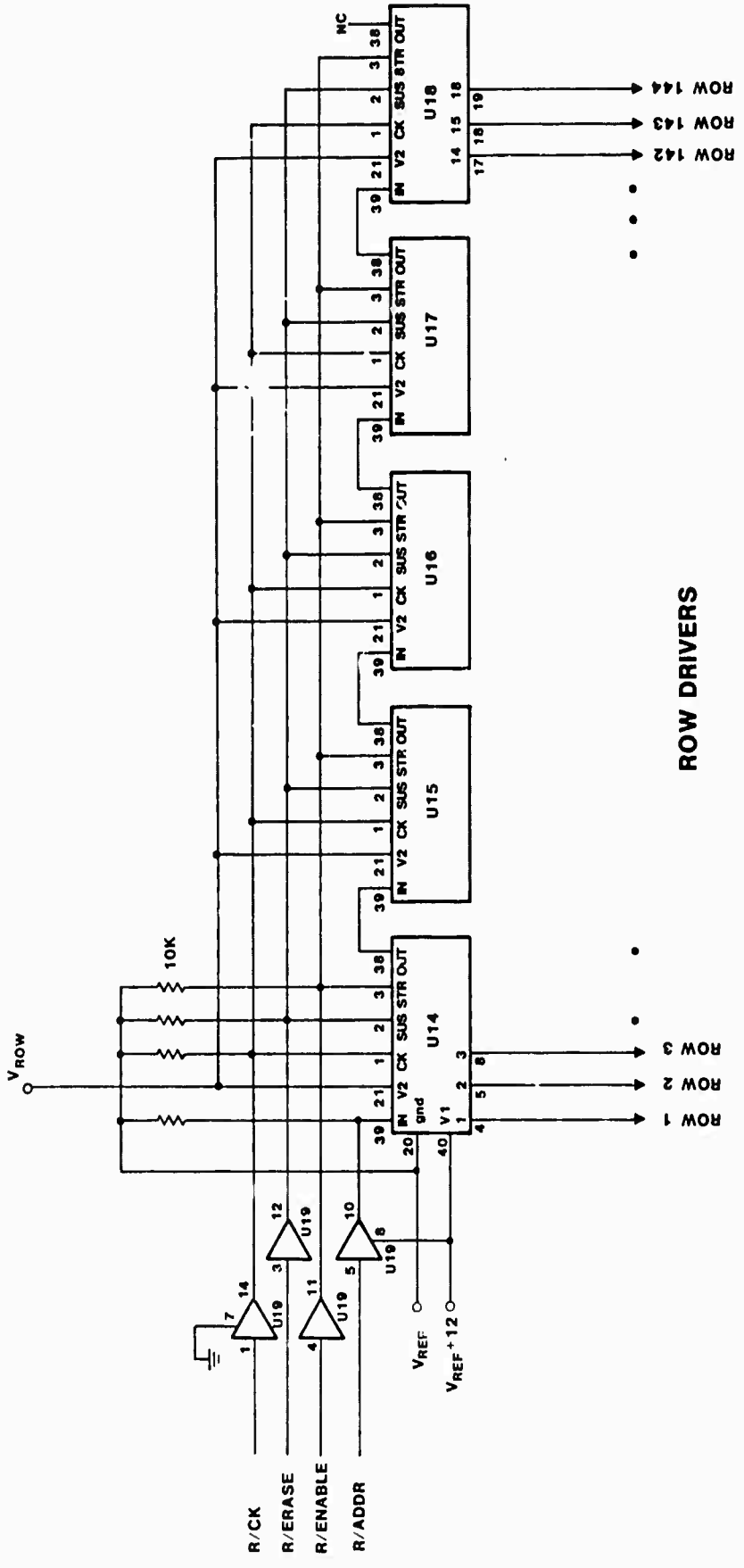

Figure 4. Circuit diagram for row driver.

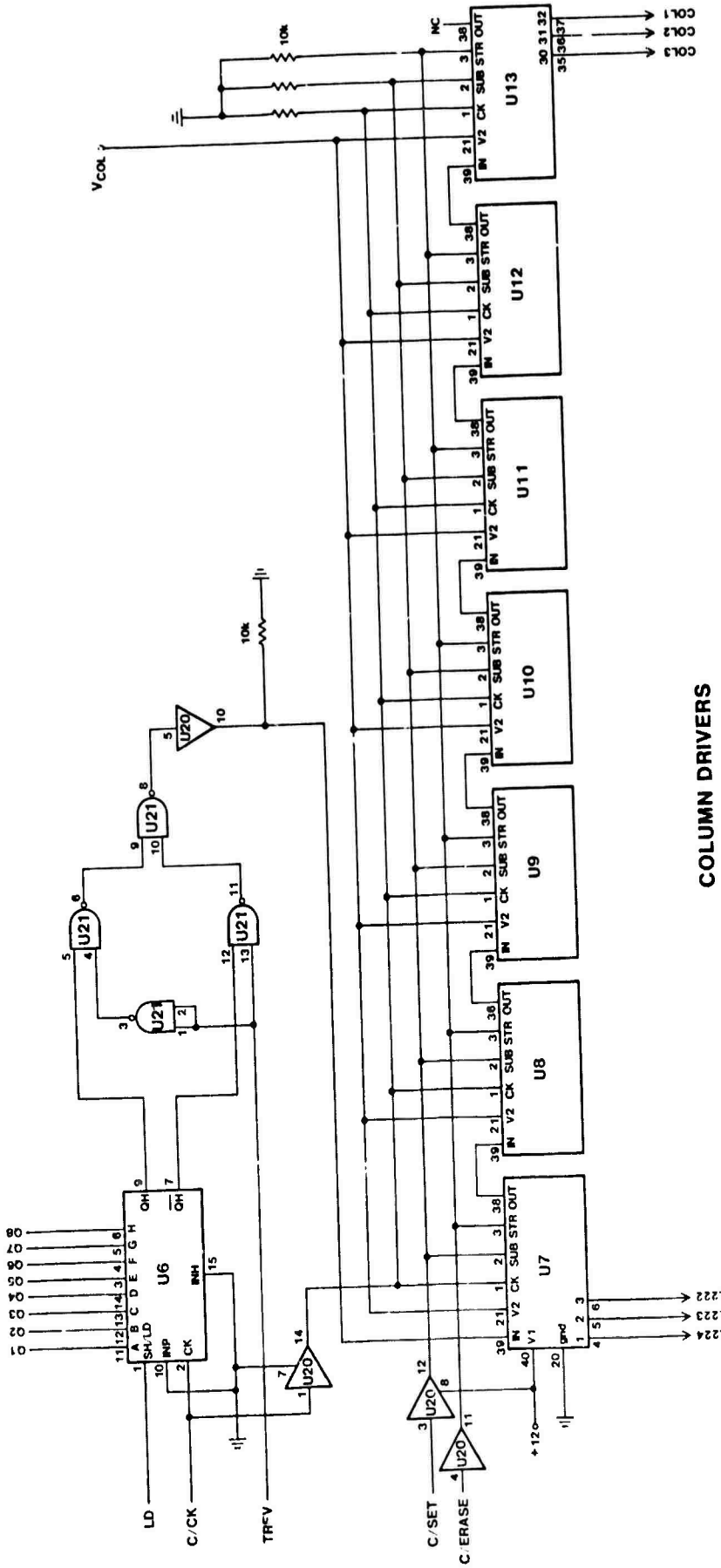

Figure 5. Circuit diagram for column driver.

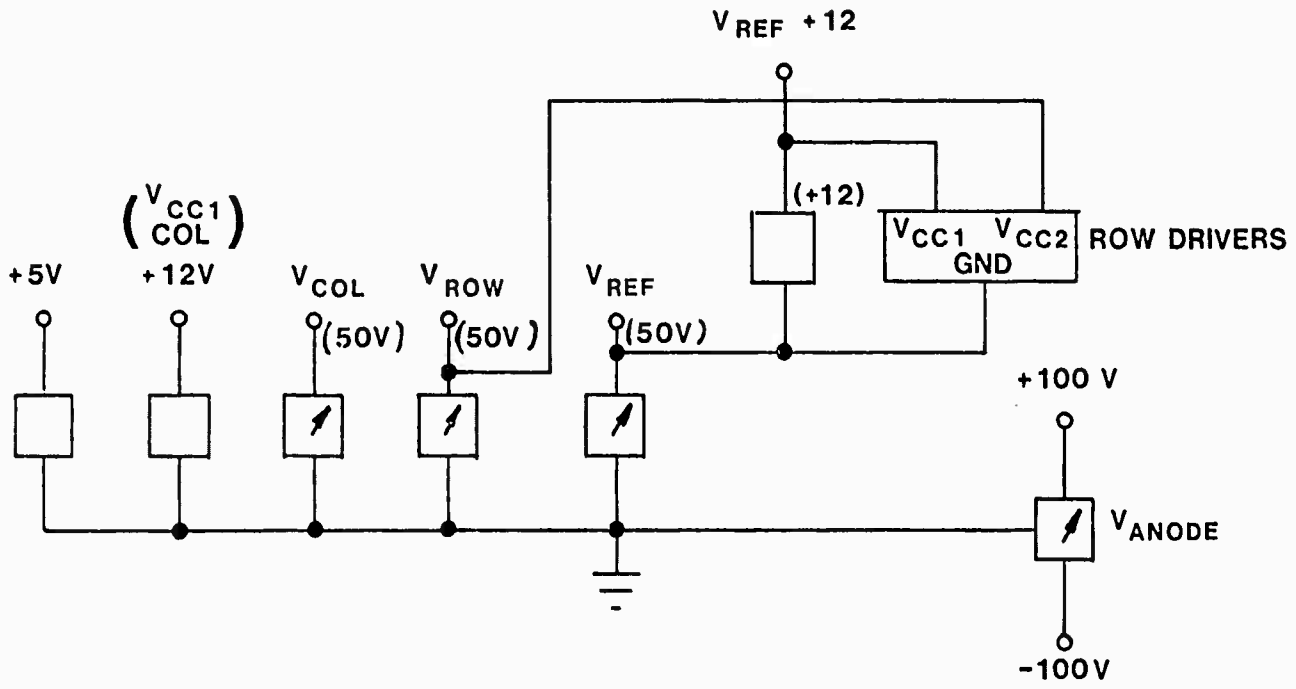

Figure 6. Power supply circuit diagram.

3.3 Packaging

The artwork for the display mounting board has been completed and approved. This board will be 7 inches by 7.5 inches and will fan out the 228 column contacts, the 148 row contacts and the 4 redundant anode contacts to eight sockets. Figure 7 shows the artwork for this board.

The components for the driver will be mounted on two 9 inch by 9 inch boards and interconnected by wire-wrap. These two boards will be mounted along with the modular power supplies in a single cabinet. Ribbon cables will connect the driver to the display mounting board.

4. PLANS FOR NEXT QUARTER

a. Characterize ITO sputtering system.

b. Fabricate devices with ITO grid electrodes using improved methods.

c. Complete construction and packaging of driver.

d. Program and debug driver.

e. Display α-N information on a device with ITO grid electrodes.

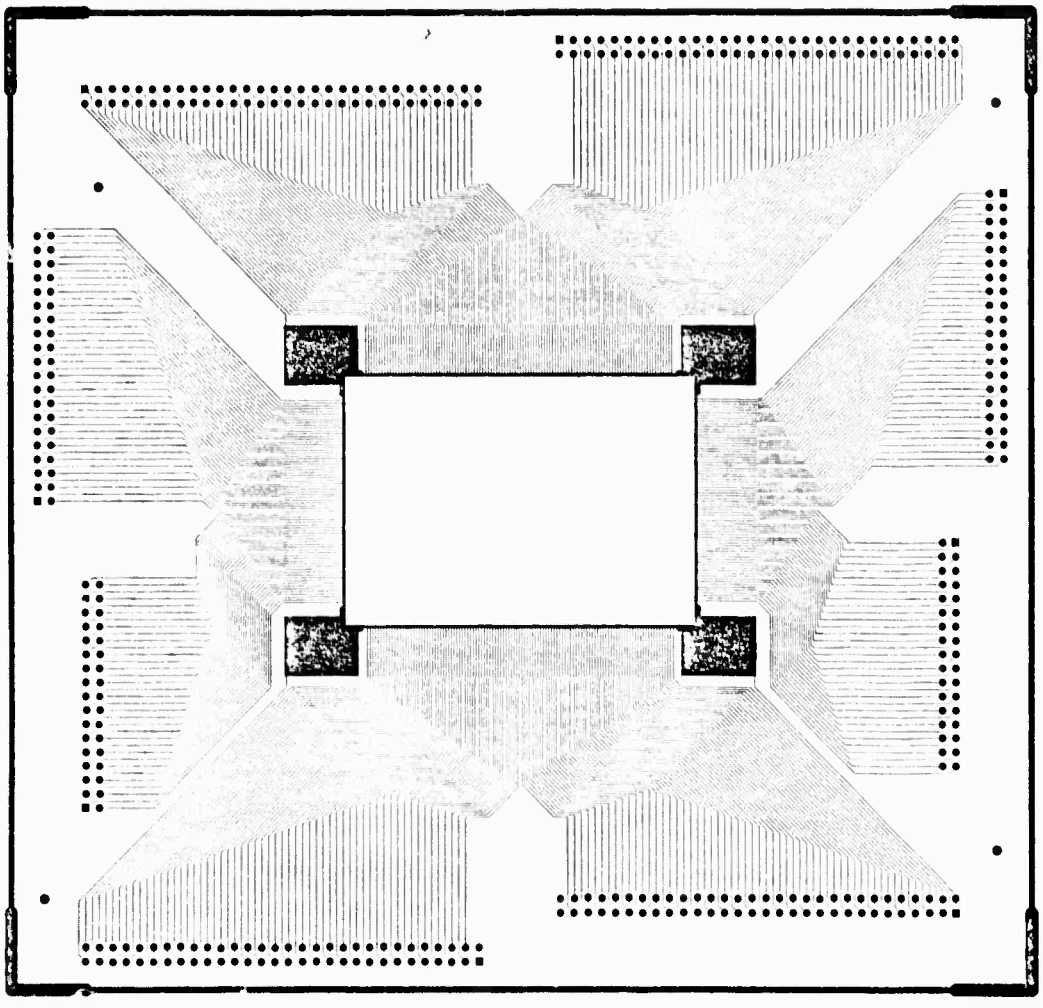

Figure 7. Artwork for display mounting board.

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